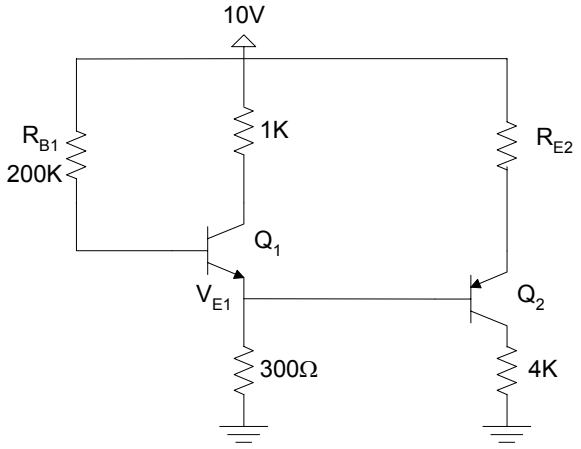
EECE 310 – SAMPLE BJT PROBLEMS

- Unless otherwise specified, assume that:

- $V_T = 25$ mV
- $|V_{BE(ACTIVE)}| = 0.7$ V
- $|V_{CE(SAT)}| = 0.2$ V
- $\beta = 100$

- Capacitors are very large
- Body effect, Early effect, and channel-length modulation are negligible

1.
In the circuit shown below, assume $V_{E1} = 2.5$ V, $\beta_1 = 100$ for the NPN BJT, and $\beta_2 = 20$ for the PNP BJT. Calculate I_{B1} in μA.
a) 34 b) 29 c) 39 d) 31.5 e) 36.5

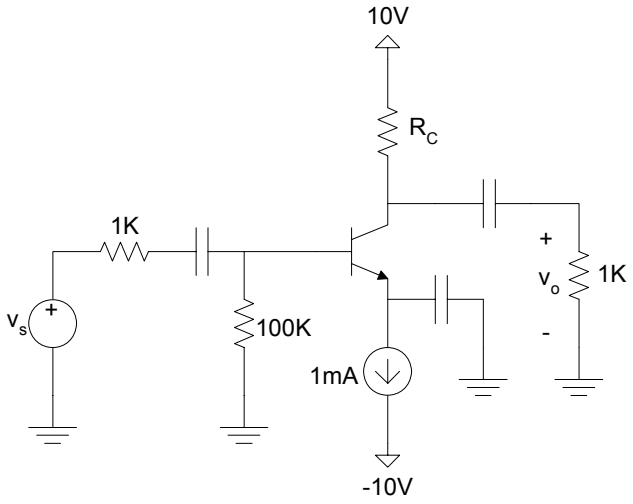


2.
In problem 1, find V_{C1} in V.
a) 6.35 b) 6.1 c) 6.6 d) 6.85 e) 7.1

3.
In problem 1, find I_{E2} in mA.
a) 7.69 b) 1.56 c) 3.61 d) 5.65 e) 9.74

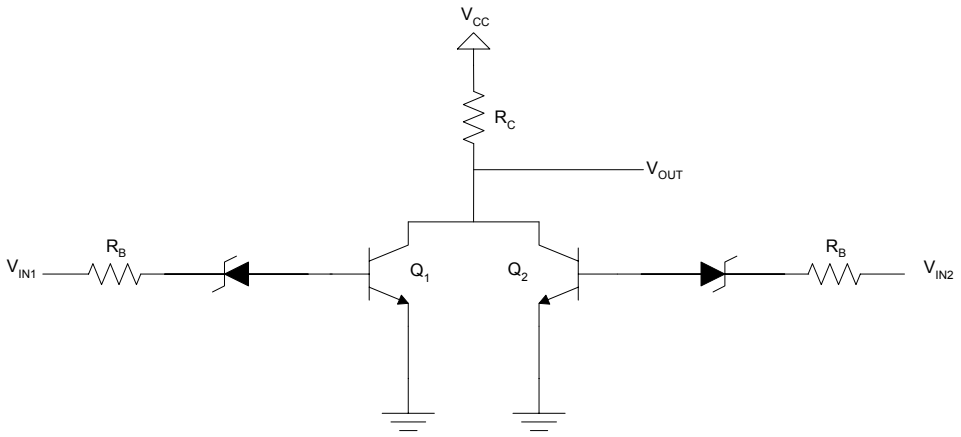
4.
In problem 1, find R_{E2} in KΩ.
a) 0.819 b) 5.00 c) 0.596 d) 2.02 e) 1.20

5.
For the BJT amplifier shown below, find V_{CE} in V. Assume $R_C = 2500$ Ω.
a) 10.2 b) 9.71 c) 8.72 d) 9.21 e) 8.22



6.
Find the voltage gain v_o/v_s in problem 5.
a) -21.1 b) -21.9 c) -16.9 d) -18.8 e) -20.1

7.
Find the logic function of the RTL gate shown below. Assume V_{CC} = 12 V, R_C = 1 KΩ , R_B = 10 KΩ, and that the Zener diodes drop 4.7 V when conducting.
a) NAND b) NOR c) AND d) NOT e) OR



8.
Find the output level (in V) that corresponds to LOW in the gate of problem 7.
a) 0.5 b) 0.7 c) 1.2 d) 0.2 e) 1

9.
Find the output level (in V) that corresponds to HIGH in the gate of problem 7.
a) 12 b) 11.3 c) 6.6 d) 4.7 e) 15

10.
Find the power drawn by the gate (in W) from the V_{CC} power supply when only one input is high in the circuit of problem 7.
a) 0.0118 b) 0.222 c) 0.142 d) 2.05 e) 0.0148

11.
Find the value of V_{IL} (in V) for the gate of problem 7. The value of V_{IL} in this case is approximated by the value of input voltage at which the BJT starts conduction (the BJT is at the edge of the active region.)

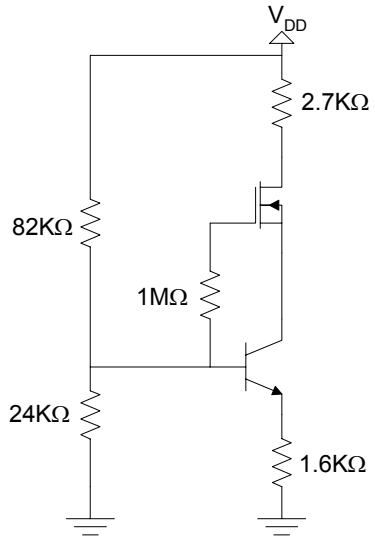
a) 0.7 b) 5.4 c) 1.4 d) 12 e) 4.7 V

12.
Find the base current of Q_1 (in mA) in the circuit of problem 7, when Q_1 is at the edge of the saturation region. Assume that V_{IN2} is low.
a) 0.841 b) 0.075 c) 0.118 d) 0.148 e) 0.536

13.
Find the value of V_{IH} (in V) for the gate of problem 7. The value of V_{IH} in this case is approximated by the value of input voltage at which the BJT is at the edge of saturation.
a) 6.58 b) 5.58 c) 6.88 d) 5.88 e) 8.55

14.
Find the base current of Q_1 (in mA) in the gate of problem 7 when the input voltage is $V_{IN1} = 7$ V. Assume that V_{IN2} is low.
a) 0.06 b) 0.16 c) 0.26 d) 0.36 e) 0.46

15.
In the circuit shown below, the MOSFET is N-channel *depletion* with $k'(W/L) = 1$ mA/V^2 and $V_t = -6$V. Find the base current of the BJT in μA. Assume $V_{DD} = 16$ V.
a) 14.96 b) 12.45 c) 11.19 d) 13.71 e) 16.22



16.
In problem 15, find the collector voltage (in V) of the BJT.
a) 7.13 b) 7.39 c) 7.01 d) 7.26 e) 7.52

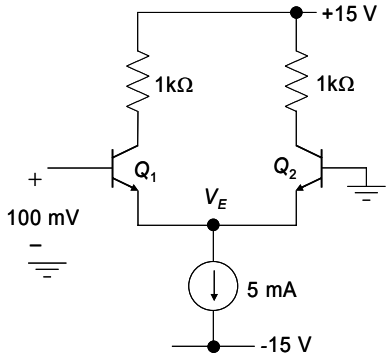
17.
A CMOS inverter powered by a $V_{DD} = 2.5$ V supply uses an N-channel MOSFET with $k'_N(W/L)_N = 2$ mA/V^2, $V_{tn} = 0.7$ V, and a P-channel MOSFET with $k'_P(W/L)_P = 1$ mA/V^2, $V_{tp} = -0.8$ V. Find the output LOW voltage level (in V)
a) 0.076 b) 0.131 c) 0 d) 0.101 e) 0.128

18.
The inverter in problem 17 is loaded by a load that sources 1 mA from V_{DD} *into the output*. What is the output voltage (in V) in this case? The input is HIGH.
a) 0.303 b) 0.185 c) 0.155 d) 0.229 e) 0.134

19.
What is the dynamic power dissipation (in mW) of the CMOS inverter in problem 17 when it is loaded by a 1 pF capacitor and its input is a 16 MHz clock.
a) 0.324 b) 0.1 c) 0.256 d) 0.144 e) 0.196

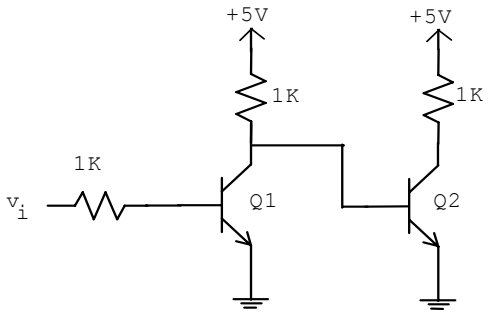
20.
The propagation delay of the CMOS inverter in problem 17 is 1 ns when loaded by a 1 pF capacitor. What happens to the propagation delay when the load capacitance is reduced to 0.5 pF? The delay is
a) unchanged b) increased to 2ns c) reduced to 0.5 ns
d) increased to 4 ns e) reduced to 0.25 ns

21.
In the circuit shown below, the transistors are identical, have *very large* β, and V_{BE} = 0.68 V at I_E = 1 mA. Determine the value of V_{BE} when I_E = 4 mA.
a) 0.69 V b) 0.71 V c) 0.73 V d) 0.67 V e) 0.75 V



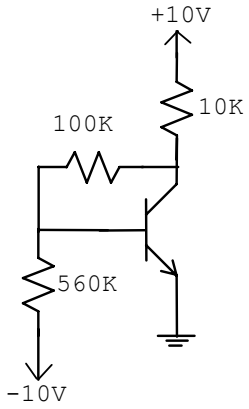
22.
Determine V_E with respect to ground in the circuit of problem 21.
a) –0.63 V b) –0.64 V c) –0.66 V d) –0.62 V e) –0.65 V

23.
For the circuit shown, in what region of operation are the two BJTs operating when v_i = 5 V? Assume β_{min} = 10.



24.
In the circuit shown below, assume $\beta = 99$.

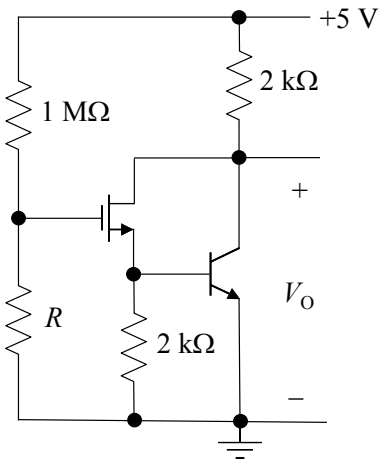
a) Find the base current of the BJT.
b) Find the value of V_{CE}.



25.
A 10 KΩ resistor is connected between the output of a CMOS inverter and ground. Find the resulting value of V_{OH} (when the input is zero volts.) Assume $V_{DD} = 5$ V, $V_{tn} = -V_{tp} = 1$ V, and $k'_n(W/L)_n = k'_p (W/L)_p = 0.1$ mA/V^2.

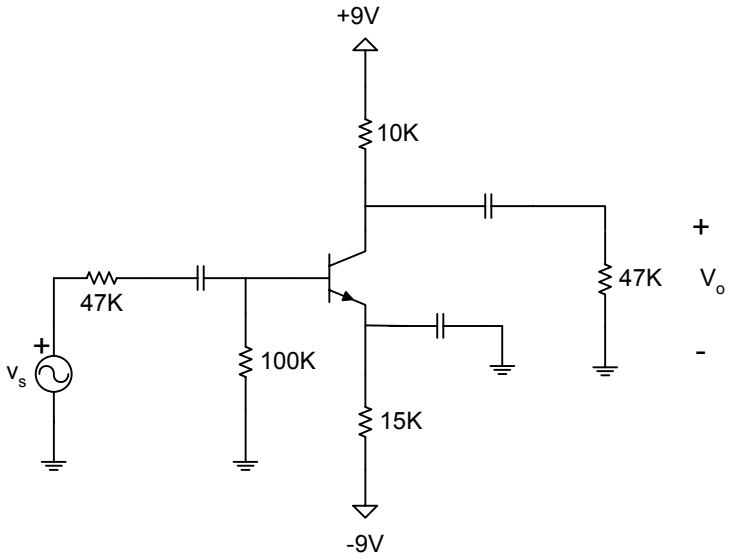
26.
Refer to the circuit shown on the right. Determine R so that the DC output $V_O = 2$ V, assuming β to be *very large*, $V_{BE} = 0.8$ V, $k'_n(W/L) = 0.2$ mA / V^2, and $V_t = 1$ V.

a) 4.36 MΩ b) 3.17 MΩ
c) 10.54 MΩ d) 6.14 MΩ
e) none of the above



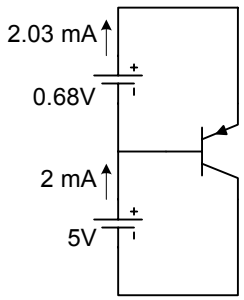
27.
In the previous problem, find the collector current of the BJT.
a) 1.5 mA b) 0.5 mA c) 1.1 mA d) 2.1 mA e) none of the above

28.
Consider the BJT amplifier shown below. The BJT has $V_A = 75$ V.

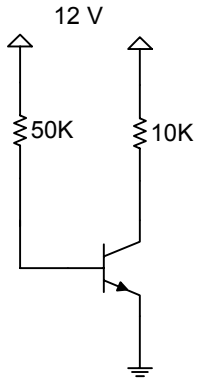


a) Find the value of α for this BJT.
b) Perform a DC analysis to determine: I_B, I_C, I_E, V_{BE}, V_{BC}, V_{CE}. Neglect the Early effect in the DC analysis. Verify your assumptions.
c) Find the small signal quantities g_m, r_π, r_e, and r_o.
d) Find the voltage gain of this amplifier, v_o/v_s
e) If v_{be} is limited to 10 mV peak-to-peak, find the maximum peak-to-peak variation in the collector voltage. Would the BJT remain active for such peak-to-peak variation in collector voltage? What is the corresponding peak-to-peak variation in v_s?
f) Find the maximum peak-to-peak variation in collector voltage to keep the BJT active. Neglect distortion.

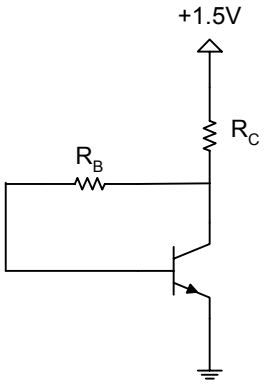
29.
For the BJT shown in the circuit, determine the values of β and I_S.



30.
In what region is the BJT shown in the circuit operating? Assume that β varies between 50 and 200. Justify your answer.

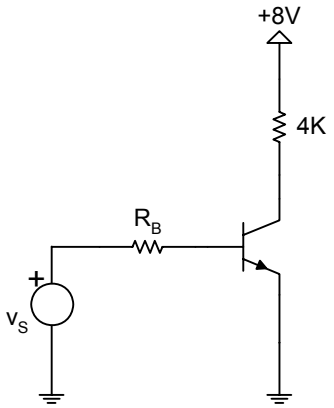


31.
a) Design the bias circuit in the figure below (find the values of R_B and R_C) to get a collector current of 10 μA and a collector voltage of 0.9 V. Assume that β = 60.



b) If β of the BJT happens to be 120, find the new Q point (I_C, V_{CE}). Use the values of R_B and R_C that you found in part (a).

32.
For the BJT amplifier shown below, the source v_S establishes a DC base current of 10 μA. In addition, the source causes a sinusoidal signal current component i_b of 10 μA *peak-to-peak* to appear in the base, and a sinusoidal signal voltage component v_{be} of 20 mV *peak-to-peak* to appear between base and emitter.



From the graphical characteristics of the BJT shown below, use the load line to find the Q point (I_C, V_{CE}). What is the value of β for the BJT, at the Q point?

Given the signal component i_b, determine, graphically, the signal components in i_C and v_{CE}. Mark all your points on the graph.

Determine the following quantities: voltage gain v_{ce}/v_{be}, current gain i_c/i_b, and i_c/v_{be}. What does this last quantity (i_c/v_{be}) represent? Give an estimate of the value of the Early voltage V_A for this BJT, around the Q point.